EE-241. Introductory Electronics Laboratory
Lab 11 Handout*

Fall 2009

Due Date: Dec 9th, 2009

1 Background

1.1 Summary of MOSFET operation

In Lab 8, we used an NMOS device as a switch. Let us recall its operation. On applying positive voltage at the gate terminal, an electric field is created which controls the current flowing from the drain to the source in the channel. To summarize our observations from the lab, the NMOST device operates in the following regions.

Cutoff. $V_{GS} < V_t$

Triode. $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$

Saturation. $V_{GS} > V_t$ and $V_{DS} > V_{GS} - V_t$

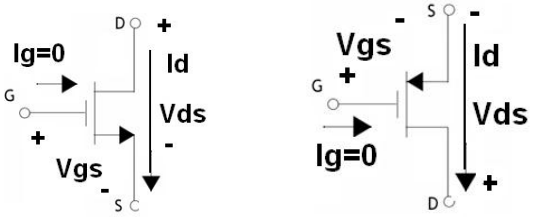
For a PMOS device, the regions are as follows.

Cutoff. $V_{GS} > V_t$

Triode. $V_{GS} < V_t$ and $V_{DS} > V_{GS} - V_t$

Saturation. $V_{GS} < V_t$ and $V_{DS} < V_{GS} - V_t$

Note that for a PMOS device; V_{GS}, V_{DS} and V_t are all negative.



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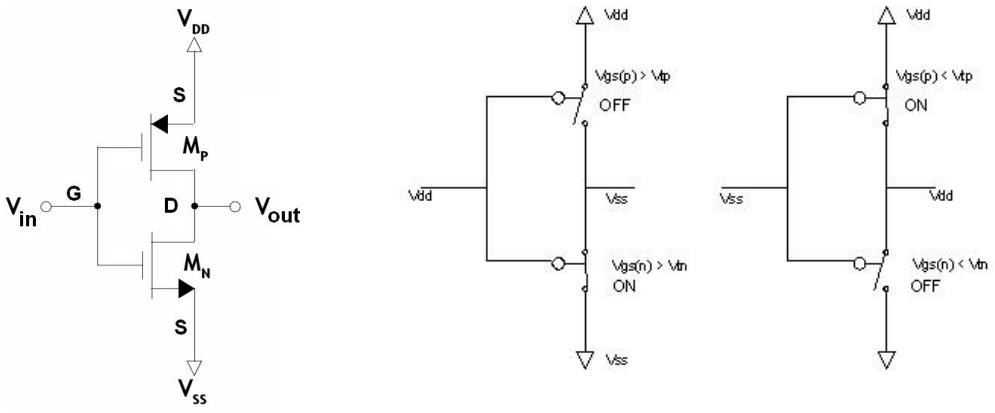
1.2 CMOS Logic Gates

In this exercise, we will study how CMOS (Complementary metaloxidesemiconductor) technology for constructing integrated circuits (IC) works. CMOS is one of the most commonly used IC technology in microprocessors, memories, imaging sensors, communication circuits and data converters. They are ideal due to their low power consumption and high noise immunity. CMOS is based on MOSFETS. The word *complementary* in CMOS indicates the use of NMOS and PMOS transistors as pairs in the same circuital unit. The transistors are arranged in CMOS circuits in the following way: all PMOS transistors must have either an input from the voltage supply or from another PMOS transistor. Similarly, all NMOS transistors must either have an input from ground or from another NMOS transistor. We begin by studying how to make the simplest logic gate using CMOS technology.

1.3 CMOS Inverter Gate

A schematic of a simple CMOS inverter is given in the Figure below. M_P is a PMOS device and its source is connected to the positive supply and M_N is a NMOS device its source is connected to the negative supply. Gates of the devices are connected together to feed V_{in} and the drains of both the transistor are connected together which serves as an output terminal of the inverter. You can assume that V_{SS} is at ground.

One can model the transistors as voltage-controlled switches. When the input voltage (gate voltage) is at V_{DD}, the NMOS transistor turns ON and shorts the output to V_{SS}, a lower voltage. In this way, we apply a high voltage as the input (logical high 1) and we get a negative output (logical low 0). Similarly on applying V_{SS} at the input, the PMOS device turns ON and shorts the output to V_{DD}. This explains the operation of this circuit as a digital inverter.



1.4 Inverter Voltage Transfer Characteristic Curve

Figure 1.4 shows the voltage transfer characteristic curve (VTC) of a CMOS inverter. If both the transistor are matched then we can assume that both transistors have the same threshold voltage. The curve is divided into the following regions as V_{in} is increased from 0.

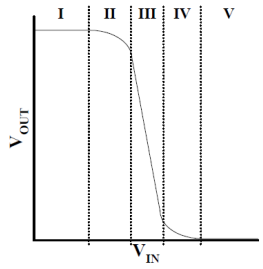
Region I: When $V_{in} < V_t$. NMOS is in cutoff and PMOS in triode region. A low-resistance path from V_{DD} to V_{out} pulls the output to logical *high*.

Region II: When $V_{in} > V_t$. NMOS enters saturation but PMOS stays in triode. Current flows and V_{out} starts to fall.

Region III: High-gain region. Both NMOS and PMOS are saturated. The slope of VTC is the voltage gain.

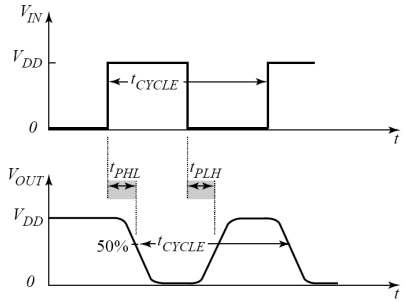
Region IV: NMOS enters triode while PMOS stays in saturation.

Region V: When $V_{in} > V_{DD} - V_t$. PMOS is in cutoff and NMOS is in triode. A low resistance path is created from V_{out} to ground which pulls the output to logical *low*.



1.5 Propagation Delays

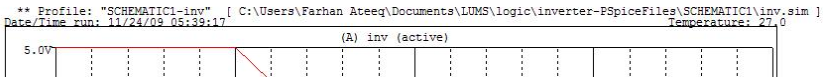
Propagation delay is the time delay between input and output signals in a logic circuit. For digital systems, this is a key figure of merit. Imagine a cascade of many invertors connected one after the other. If there is a significant delay between the input and output of each gate, then the total delay may become unacceptably large. Therefore, the propagation delay has to be as low as possible in a fast switching circuit. The delay is calculated by taking the average of the delay for a High to Low transition, and the that of a Low to High transition.



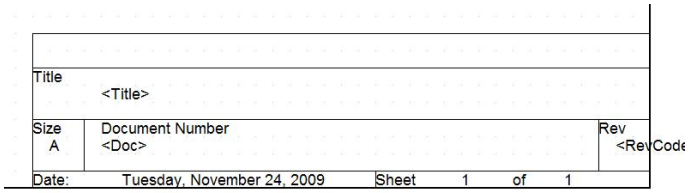
2 SPICE Exercises

2.1 Instructions

Your plot should clearly state your file name, directory path ,date/time as shown.



In the bottom right of your schematic window of OrCAD you will see a box as shown. Double click on "Title" and in the value field write your name. For Document Number write the question number. You will have to include this box in all of your schematics. Schematics handed in without your proper information will not be graded.



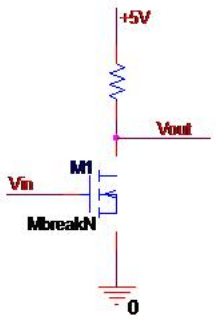
1. Build a CMOS inverter circuit in SPICE. Set V_{DD} at 5V and V_{SS} at 0V. Connect a 100nF capacitor at the output as your load. Run appropriate simulations to obtain a voltage transfer characteristic curve.

   Circuit schematic [5 marks] Simulated Plots [5 marks]

2. Apply a 2.5kHz square wave of peak-to-peak amplitude 5V to the input of the inverter. You may need to add a DC offset of 2.5V to achieve correct logic levels. Use the SPICE oscilloscope to plot the signals V_{in} and V_{out} on top of each other. Measure the propagation

delays, t_{PLH} and t_{PHL}, of the inverter. Now try this for other smaller and bigger values of frequency. Does the propagation delay change? [5 marks]

3. Consider the circuit below. Explain, how does it act as an inverter? [2 marks] Based on your answer, qualitatively what should be the value of the resistor? [2 marks]



4. Now build this circuit in SPICE. Choose an appropriate value of the resistor. You may consider any voltage less than 1V as logical "0". Again, connect a 100nF capacitor at the output as your load. Plot its simulated VTC.

   Circuit schematic [3 marks] Simulated Plots [3 marks]

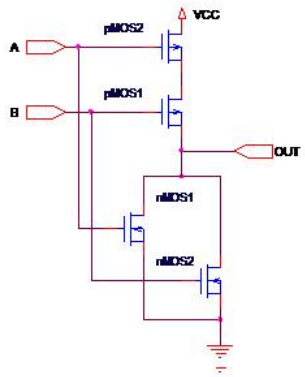
5. Apply a 250Hz square wave with the appropriate DC shift to the input of this inverter. Plot the signals V_{in} and V_{out} and measure the propagation delays, t_{PLH} and t_{PHL}. Compare the performance of this inverter against the CMOS inverter. Feel free to try other values of frequency to get a clear graph. [5 marks]

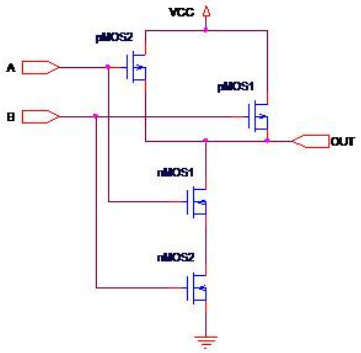
6. Build the circuit below-left in SPICE and fill in the following *truth table* after simulating its operation for various input combinations of A and B. We call the voltage level V_{DD} to be "1" or High and GND to be "0" or Low.

A	B	OUT
0	0	
0	1	
1	0	
1	1	

Can you name this logic gate? Explain how this circuit works.

Circuit schematic [3 marks] Explanation [2 marks]





7. Repeat the analysis of Q6 for the circuit on your right. Name this logic gate and explain how this circuit works.

   Circuit schematic [3 marks] Explanation [2 marks]

8. Now connect the output of the CMOS inverter from Q1 to one of the inputs of the circuit in Q6. Keep the other input at $0V$. What should be the truth table of this new circuit? [3 marks]

9. Next, apply the square wave of Q2 to the input of the circuit in Q8. Measure the total propagation delay at the output. How do you explain this new delay? [2 Marks]